REMARKS

Claims 3-5 are pending in this application. By this amendment claims 3 and 4 are amended. These amendments are supported by Applicants specification at least at, page 4, lines 29-30. No new matter is added. Reconsideration of the application based on the above amendments and the following remarks is respectfully requested.

Entry of the amendments is proper under 37 CFR §1.116 because the amendments: (a) place the application in condition for allowance for the reasons discussed below; (b) do not raise any new issue requiring further search and/or consideration as the amendments clarify features in the claims and amplify issues previously discussed throughout prosecution; (c) satisfy a requirement of form Applicant discovered in preparing this response; and (d) place the application in better form for appeal, should an appeal be necessary. The amendments are necessary and were not earlier presented because they are made in response to arguments raised in the final rejection that misconstrue the totality of the claim language. Entry of the amendments is thus respectfully requested.

The Office Action rejects claim 4 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 7,009,200 to Tezuka et al. (hereinafter "Tezuka"). This rejection is respectfully traversed.

Without conceding the appropriateness of the rejection, and solely to advance prosecution of this application, claim 4 is amended. Tezuka does not teach the combination of the features recited in this claim for, at least, the following reasons.

Tezuka teaches, at *e.g.*, col. 2, lines 48-50, the first embodiment is a P MOSFET which has a strained-$Si_{1-x}Ge_x$ layer 20 as a channel formed on a SiO_2 film 12 as shown in Fig. 1A; at col. 4, lines 25-27 in the second embodiment, a strained-Si layer 52 is formed on a lattice-relaxed $Si_{1-x}Ge_x$ layer 51 formed similarly to the first embodiment and nMOSFET is further formed on the Si layer 52; and at col. 7, lines 10-14, the MOSFET according to the seventh

embodiment is a PMOSFET which comprises the strained-SiGe layer 20 as a channel on the Si layer 15 formed on the buried oxide film 12, and is characterized in that the source and drain are lattice-relaxed Si. Other embodiments of Tezuka comprise similar layers on the buried oxide layer 12. Further, Tezuka teaches at col. 3, lines 58-60. Then, BF_2 ions are implanted to form an extension region 37 of the source and drain as shown in Fig. 2E and, at *e.g.*, col. 2, lines 64-67. Furthermore, BF_2 ions are implanted, and pulse annealing is performed for a second at 1,050°C to make impurity of the source and drain regions 34 and 35 and gate 32 activated. Thus, Tezuka teaches that the source and drain of any of the disclosed embodiments are made from the same materials implanted at the same time with the same impurities and annealed at the same at the same temperature. Accordingly, the source and drain in each of the embodiments disclosed in Tezuka are necessarily of the the same material. Tezuka does not teach, nor would it have suggested, that the source material and the drain material are different materials, as recited in claim 4.

In view of the above, Tezuka cannot reasonably be considered to teach, or to have suggested, the combination of all of the features positively recited in claim 4.

Accordingly, reconsideration and withdrawal of the rejection of claim 4 under 35 U.S.C. §102(e) as being anticipated by Tezuka are respectfully requested.

The Office Action rejects claims 3 and 5 under 35 U.S.C. §103(a) over Tezuka in view of U.S. Patent No. 4,885,614 to Furukawa et al. ("Furukawa") and U.S. Patent No. 2,918,396 to Hall. This rejection is respectfully traversed.

Without conceding the appropriateness of the rejection, and solely to advance prosecution of this application, claim 3 is amended. As argued above, Tezuka does not teach, nor would it have suggested, the source material and the drain material are different materials, as recited in claim 3.

Furukawa teaches a semiconductor device comprising a first semiconductor layer being made of a monocrystalline semiconductor material comprising silicon as the main component and the second semiconductor layer of monocrystalline semiconductor material which is obtained by incorporating carbon into a silicon-germanium alloy. Further, Furukawa teaches a modulation doped field effect transistor (see *e.g.*, col. 5, lines 41-42) and, at *e.g.*, col. 5, lines 61-65, the resulting substrate is taken out of the MBE system and subjected to photoetching, followed by the formation of source and drain electrodes 54 and 55 and a gate electrode 56 according to a conventional method, thus, a MOSFET of p channel is produced. Furukawa does not teach that the source and drain of the MOSFET are made from different materials.

Hall teaches an improved process for forming alloyed electrical contacts to silicon carbide crystals; to provide an improved process for forming rectifying alloyed and recrystallized junctions in silicon carbide crystals; and high temperature semiconductive devices (see *e.g.*, col. 1, lines 62-69). Hall does not teach the source or drain of a field effect transistor are of different materials.

Thus, a combination of Tezuka with Furukawa and Hall does not teach, nor would it have suggested, the source material and the drain material are different materials, as recited in claim 3.

As indicated by the Examiner on page 5, lines 14-16, electronic affinity is a material property which is different for different materials. Claim 5 recites, among other features, an electronic affinity of the NMOS drain material is lower than an electron affinity of the NMOS channel material and an electron affinity of the end moss source material is higher than the electronic affinity of the NMOS channel material. Thus, the electronic affinity of the source and drain materials of the NMOS transistor, recited in claim 5, are different. Therefore, the materials of the source and drain of the NMOS transistor recited in claim 5 must also be

different. As argued above, a combination of Tezuka with Furukawa and Hall does not teach the source material and the drain material are different materials, as is necessary to thhe structure of claim 5. Accordingly, the combination of Tezuka with Furukawa and Hall cannot reasonably be considered to have suggested the combination of all of the features positively recited in claim 5.

The Office Action does not adequately show that one of ordinary skill in the art would have predictably combined any feature disclosed in Tezuka with Furukawa and Hall with any reasonable expectation of success to make an NMOS or PMOS transistor in which the source material and drain material are different materials.

In view of the above, the combination of Tezuka with Furukawa and Hall cannot reasonably be considered to have suggested the combinations of all of the features positively recited in claims 3 and 5.

Accordingly, reconsideration and withdrawal of the rejection of claims 3 and 5 under 35 U.S.C. §103(a) over Tezuka in view of Furukawa and Hall are respectfully requested.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 3-5 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

William P. Berridge
Registration No. 30,024

Daniel A. Tanner, III
Registration No. 54,734

WPB:MIL/add

Date: August 4, 2008

OLIFF & BERRIDGE, PLC
P.O. Box 320850
Alexandria, Virginia 22320-4850
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461